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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/015,749	12/17/2001	Kazuhiro Sonoda	35.C16029	2844
5514	7590	11/04/2004	EXAMINER	
FITZPATRICK CELLA HARPER & SCINTO 30 ROCKEFELLER PLAZA NEW YORK, NY 10112			VILLECCO, JOHN M	
			ART UNIT	PAPER NUMBER
			2612	

DATE MAILED: 11/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/015,749	Applicant(s) SONODA ET AL.	
	Examiner John M. Villecco	Art Unit 2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 June 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 24-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 24-27 is/are rejected.
- 7) ☒ Claim(s) 27 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 December 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 18, 2004 has been entered.

Response to Amendment

2. Applicant has amended claim 24 to include a limitation that was previously not considered. Thus a new grounds of rejection is presented below.

Claim Objections

3. Claim 27 is objected to because of the following informalities:

- In line 5 of claim 27, applicant recites the phrase “the signal processing”. It appears that the applicant has inadvertently omitted the word – circuit – from the phrase and that the applicant meant to use the phrase – the signal processing circuit –.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. **Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Terui et al. (U.S. Patent No. 6,333,760) in view of Takagi et al. (U.S. Patent No. 6,795,120).**

6. Regarding *claim 24*, Terui discloses an image pickup area (11A) disposed on a semiconductor substrate (col. 2, line 27), image pickup area includes a pixel area with pixels arranged two-dimensionally, and a plurality of peripheral circuits arranged on opposite sides of the image pickup area (11A). One of the peripheral circuits includes a drive circuit (12A). The drive circuit (12A) performs predetermined processing for the pixel area. Another of the peripheral circuits includes a signal processing circuit (14A) which performs predetermined processing on the signal output from the amplifier (11-2). The amplifier is provided in common to the pixel area for outputting the pixel signals to the signal processing circuit (14A). Each of the processing circuits performs predetermined processing on the same pixel area (11A).

While Terui does disclose using a lens to focus the incoming light onto the CCD (see Figure 5), Terui fails to disclose that the lens and image pickup element are integrated into one unit. Meyers, on the other hand, discloses that it is well known in the art to integrate a lens and image pickup device into one unit. More specifically, Meyers discloses a lens (12) bonded to the integrated circuit. The addition of a lens into an image sensor package provides for a compact

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package with incoming light accurately focused onto the images sensor. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a lens into an image sensor package so that the incoming light is accurately focused onto the image sensor.

7. As for *claim 25*, Terui discloses two signal processing circuits (14 and 15) for processing signals from the image pickup element and a memory (13) for storing the data from the signal processing circuit.

8. **Claims 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Terui et al. (U.S. Patent No. 6,333,760) in view of Takagi et al. (U.S. Patent No. 6,795,120) and further in view of Kimura (U.S. Patent No. 6,172,351).**

9. Regarding *claim 26*, as mentioned above in the discussion of claim 24, both Terui and Takagi disclose all of the limitations of the parent claim. However, neither of the aforementioned references discloses that the first and second processing circuits include one of an A/D converter, a clock circuit, an electric power source circuit, and an analog circuit.

Kimura, on the other hand discloses that it is well known in the art to include various processing circuits on opposite sides of a pixel array. As shown in Figure 10, Kimura discloses a timing generator, which would inherently include a clock circuit, and an A/D converter disposed on opposite sides of the pixel array. Kimura also discloses a signal processing portion and an analog portion in different embodiments of the invention. These circuits allow for an enhanced image output from the image sensor. Therefore, it would have been obvious to one of ordinary

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skill in the art at the time the invention was made to include the above mentioned processing circuits so that a high quality image is output from the image sensor.

10. As for *claim 27*, both Kimura and Terui disclose a signal processing circuit for processing signals from the image pickup element and a memory for storing a signal from the signal processing circuit.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9306 (For either formal or informal communications intended for entry. For informal or draft communications, please label "**PROPOSED**" or "**DRAFT**")

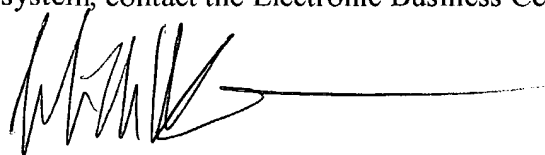
Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington VA, Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John M. Villecco whose telephone number is (703) 305-1460. The examiner can normally be reached on Monday-Thursday.

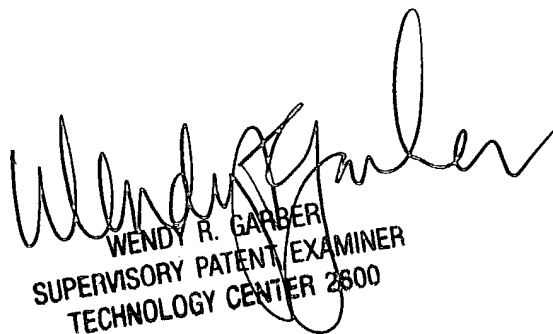
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on (703) 305-4929. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



John M. Villecco
October 26, 2004



WENDY R. GARBER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600